Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) SON-2047	
	Application Number 09/802,857-Conf. #3304	Filed March 12, 2001
	First Named Inventor Akihiko Koh et al.	
	Art Unit 2192	Examiner M. J. Yigdall

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant /inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 24,104/40,290
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

40,291
Signature

Ronald P. Kananen/Christopher M. Tobin
Typed or printed name

(202) 955-3750
*Telephone number

April 24, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[x] *Total of 1 forms are submitted.

Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Application No.: 09/802,857 | Confirmation No.: 3304

Filed: March 12, 2001 | Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM | Examiner: M. J. Yigdall

REQUEST FOR PRE-APPEAL BRIEF PANEL REVIEW OF REJECTION

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Paragraph 8 of the Office Action indicates a rejection of claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).

Claims 27-28 and 40 - While not conceding the propriety of this rejection and in order to advance the prosecution of the above-identified application, the cancellation of claims 27-28 and 40 have been proposed within the Amendment After Final Office Action under 37 CFR 1.116 of February 15, 2008.

Entry of the Amendment After Final Action and allowance of the remaining claims is respectfully requested.

Paragraph 9 of the Office Action indicates a rejection of claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki).

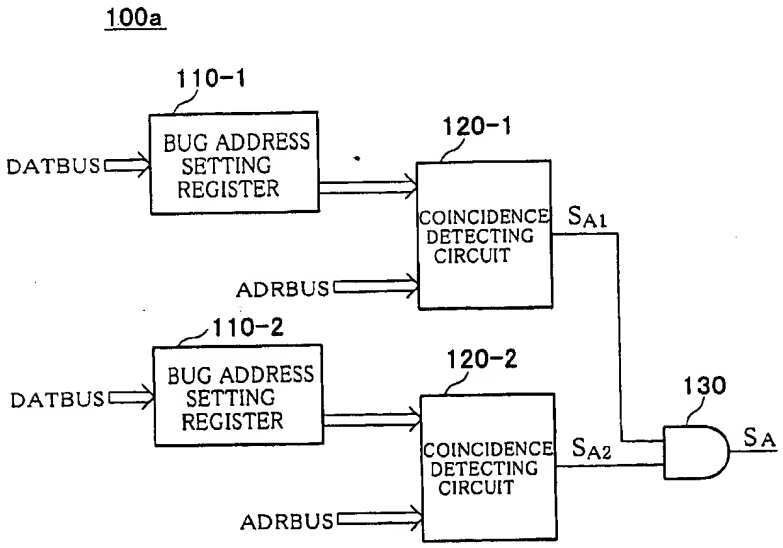
Paragraph 10 of the Office Action indicates a rejection of claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).

The ***incorporation*** in its entirety ***of claim 51 into claim 45*** has been proposed within the Amendment After Final Office Action under 37 CFR 1.116.

Prior claim 51 (which is proposed amended claim 45) is drawn to a data processing apparatus wherein said first and second interrupt request signals are ***input to said central processing unit as a single interruption***, and wherein said first and second interrupt request signals are ***AND'ed together to become said single interruption***.

Figure 7 of the specification as originally filed is shown hereinbelow.

FIG.7



U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application, provides in paragraph [0073] that:

> [0073] When there is sufficient leeway in the interrupt processing of the CPU 10, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 can be input to the CPU 10 as two different interrupt request signals. Accordingly, the CPU 10 receives these as different interrupt requests and executes the debugged programs separately to correct the two bugs. In general, however, the number of the interruptions that the CPU 10 is able to process is limited, so a plurality of bug processings have to be assigned to a single interruption. In this case, as shown in FIG. 7, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 are input to an AND gate 130, and the output signal S_A Of the AND gate 130 is input to the CPU 10 as the interrupt request signal.

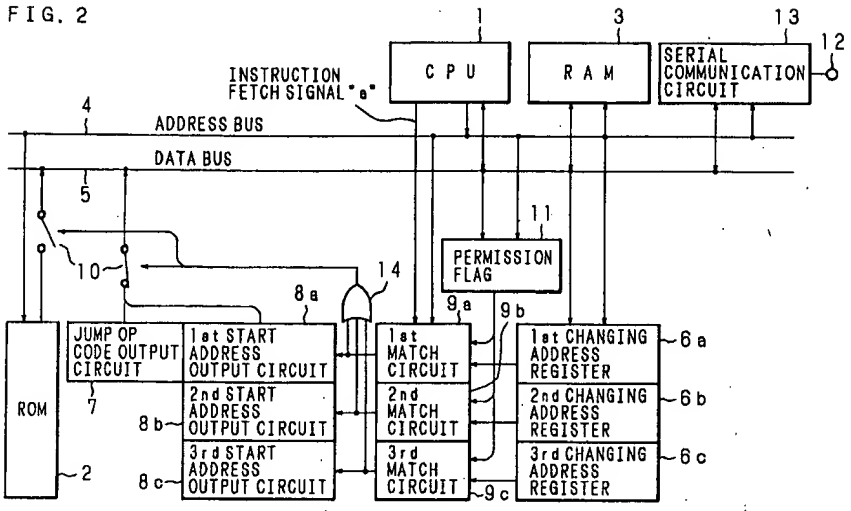
Sagane, Koscal and Suzuki - The Office Action ***admits*** that Sagane, Koscal and Suzuki *do not expressly disclose* that wherein said first and second interrupt request signals are input to said central processing unit as a single interruption (Office Action at page 18).

Hosotani - The Office Action cites Hosotani for the features that are admittedly absent from within Sagane, Koscal and Suzuki.

Hosotani arguably teaches that *the CPU 1* is also connected, via the address bus 4 and a signal line of an instruction fetch signal a, to the *first to third match circuits 9a to 9c* that respectively compare the change addresses with the address on the address bus 4 in synchronism with the output timing of the instruction fetch signal a from *the CPU 1*, and output signals indicating the results of the comparisons (a "1" level indicates an address match, and a "0" level indicates an address mismatch) (Hosotani at column 4, lines 46-53).

Figure 2 of Hosotani is shown hereinbelow.

FIG. 2



However, Hosotani ***fails*** to disclose, teach, or suggest the signals from the first to third match circuits 9a-9c being input to CPU 1.

Instead, the first to third match circuits 9a-9c are connected to a *three-input OR circuit 14* (Hosotani at column 4, lines 60-61).

However, Hosotani ***fails*** to disclose, teach, or suggest the signals from the *three-input OR circuit 14* being input to CPU 1.

Instead, ***the output of the OR circuit 14 is connected to a connection control means 10*** which selects either the mask ROM 2 or a jump op code output circuit 7 and first to third start address output circuits 8a-8c for connection to the data bus 5 in accordance with the output level of the OR circuit 14 (which outputs a "1" level when the result of comparison from any one of the match circuits 9a-9c indicates a match, and a "0" level when all the comparison results indicate a mismatch) (Hosotani at column 4, line 61, to column 5, line 2).

- ***Thus, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.***

- ***Moreover, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are AND'ed together to become said single interruption.***

Page 2 of the Advisory Action of April 9, 2008 merely offers that "the rejections are based on combinations of references".

In response, assertions of technical facts in areas of esoteric technology ***must always be supported*** *by citation to some reference work* recognized as standard in the pertinent art. *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

However, both the Final Office Action and the Advisory Action ***fail*** to identify any teaching within Sagane, Koscal, Suzuki, and Hosotani, either individually or as a whole, that is sufficient to show that *first and second interrupt request signals that are input to said central processing unit as a single interruption, the first and second interrupt request signals being AND'ed together to become the single interruption.*

Dated: April 24, 2008

Respectfully submitted,

By 40,290

Ronald P. Kananen
Registration No.: 24,104
Christopher M. Tobin
Registration No. 40,290
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorneys for Applicant